RAGO: Systematic Performance Optimization for Retrieval-Augmented Generation Serving

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Abstract

Retrieval-augmented generation (RAG), which combines large language models (LLMs) with retrievals from external knowledge databases, is emerging as a popular approach for reliable LLM serving. However, efficient RAG serving remains an open challenge due to the rapid emergence of many RAG variants and the substantial differences in workload characteristics across them. In this paper, we make three fundamental contributions to advancing RAG serving. First, we introduce **RAGSchema**, a structured abstraction that captures the wide range of RAG algorithms, serving as a foundation for performance optimization. Second, we analyze several representative RAG workloads with distinct **RAGSchema**, revealing significant performance variability across these workloads. To address this variability and meet diverse performance requirements, we propose **RAGO** (Retrieval-Augmented Generation Optimizer), a system optimization framework for efficient RAG serving. Our evaluation shows that RAGO achieves up to a 2× increase in QPS per chip and a 55% reduction in time-to-first-token latency compared to RAG systems built on LLM-system extensions.

1 Introduction

The rapid adoption of Large Language Models (LLMs) across diverse applications — spanning question answering [22, 24, 26], code generation [66, 69, 79], and scientific discoveries [19, 59, 92] — showcases their profound impact on automating knowledge-based tasks. Despite these capabilities, LLM systems, when deployed in isolation,[1] face substantial challenges, such as data staleness [55, 63], a propensity to hallucinate (generating factually incorrect or nonsensical information), and limited, often rigid model knowledge [40, 63, 67]. These challenges hinder the reliability and adaptability of LLM-only systems, especially in applications that demand high factual accuracy [28, 38, 50, 94].

Retrieval-Augmented Generation (RAG) has emerged as one powerful solution to address the common pitfalls of LLM-only systems.

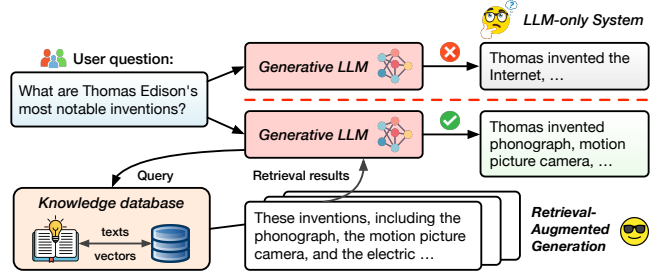[1]We refer to these systems as LLM-only systems.

Figure 1: LLM-only system (top) versus RAG (bottom).

By retrieving information from external databases and appending it to prompts (Figure 1), RAG enhances the credibility, timeliness, and contextually rich nature of LLM-generated responses. Leveraging the generative prowess of LLMs alongside external knowledge sources, RAG not only achieves comparable quality with smaller models [21, 86, 97] but also simplifies the process of updating knowledge, mitigating the extent of additional model training, which is often prohibitively expensive [55, 62]. These advantages have established RAG as the industry standard for knowledge-intensive applications, with notable examples including Google's REALM [35] and Meta's MARGE [62], RETRO [21], Microsoft's GraphRAG [27], and NVIDIA's InstructRETRO [97]. As companies race to integrate RAG systems into their production pipelines [25, 75, 85], optimizing their performance has become increasingly critical.

In contrast to conventional LLM-only serving systems, which center predominantly on optimizing the prefix (prompt decoding) and decoding (token generation) stages, RAG presents three challenges: **(C1)** RAG systems are intrinsically heterogeneous, comprising a diverse array of system components, including vector search-based retrieval [21, 63, 86], generative LLMs [22, 75, 93], and multiple optional models such as database encoders [57, 84], query rewriters [23, 72], and retrieval result rerankers [13, 31]. These components often run on heterogeneous hardware platforms. For example, retrievals are typically performed on CPU servers, whereas ML accelerators (e.g., TPUs or GPUs) are used for model serving.

This interplay of diverse components and hardware platforms amplifies the search space, far surpassing that of LLM-only systems; **(C2)** Various RAG configurations defined by factors such as database size, retrieval frequency, model selection, and serving hardware, exhibit substantial performance variability. This variability can veer the bottleneck between inference and retrieval or among different models within the serving pipeline; and **(C3)** A natural consequence of the heterogeneity in components and the variability in performance is the emergence of a new challenge: *how can we design efficient RAG serving systems?* Addressing this challenge demands meticulously navigating key decisions in scheduling policies across diverse RAG configurations and hardware platforms.

To address these challenges, we ground our approach in three key design principles: (1) **Workload abstraction**: Tackling the heterogeneity of RAG systems necessitates an abstraction to encapsulate the diverse RAG workloads. Without such abstraction, the inherent complexity of RAG configurations become intractable; (2) **Critical system design decisions**: To unveil the critical system design decisions and illuminate the performance trade-offs inherent in RAG serving, a careful performance characterization of representative RAG workloads is warranted. Without understanding how these different workloads behave, the optimization process risks becoming guesswork; and (3) **Systematic optimization framework**: To navigate the large optimization space arising from the Cartesian product of RAG workload and system design dimensions, an optimization framework is essential to uncover and exploit efficiency opportunities in RAG serving systems.

To systematically describe RAG workloads, we introduce `RAGSchema` (§3), a RAG serving abstraction that encapsulates a set of essential performance-relevant workload attributes. `RAGSchema` includes two key components: (a) specification of the RAG pipeline —document encoder, query rewriter, result reranker, and generative LLM— and (b) model and retrieval configurations, including model size, database size, the number of query vectors per retrieval, and iterative retrieval frequency. This abstraction simplifies the representation of complex RAG workloads while providing sufficient information for performance characterization and optimization.

Building on `RAGSchema`, we perform a detailed workload characterization (§5) to identify bottlenecks and key system design decisions. We analyze four representative RAG paradigms, each with distinct RAG pipeline: (a) RAG with hyperscale retrieval [21, 86, 97]; (b) RAG for long-context sequence processing [56, 68, 101]; (c) RAG with iterative retrieval [21, 45, 95]; and (d) RAG with query rewriter and retrieval reranker models [13, 23, 31, 72]. Our analysis reveal *significant performance variability both across and within paradigms*, with a subset of findings summarized as follows. First, bottlenecks shift between retrieval and inference across RAG paradigms. For instance, hyperscale retrieval can spend over 80% in retrieval (§5.1) while in long-context scenarios, retrieval accounts for less than 1% of the total latency (§5.2). Second, even smaller models within the pipeline can significantly influence system performance. For example, in long-context processing, a database encoder that is 100× smaller than the main generative LLM can become the bottleneck due to the large number of tokens it must process (§5.2). Third, iterative retrievals during decoding can stall the pipeline, as the decoding
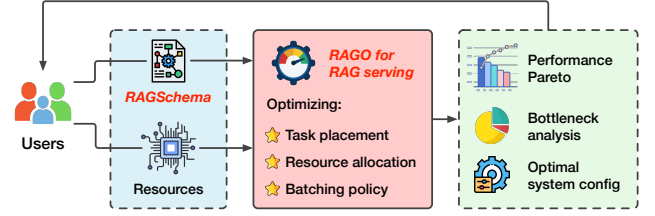

Figure 2: `RAGO` for systematic RAG serving optimization.

process waits for retrieval results (§5.3). The insights from these studies underscore not only the importance of making appropriate system design decisions but also the indispensable need for a tailored optimization framework for RAG serving systems, given their far less predictable performance landscape compared to LLM-only systems.

To this end, we introduce `RAGO` (<u>R</u>etrieval-<u>A</u>ugmented <u>G</u>eneration <u>O</u>ptimizer), a system optimization framework for efficient RAG serving (Figure 2). Given a `RAGSchema` configuration and hardware resource constraints, this framework explores the scheduling policy space to determine optimal schedules aligned with user-defined performance objectives. Key scheduling decisions of `RAGO` include deciding whether inference components are collocated or disaggregated across ML accelerators (*task placement*), assigning the type and quantity of resources to each component (*resource allocation*), and tuning batch sizes for retrieval and inference tasks to balance throughput and latency (*batching policies*). `RAGO` uses an analytical cost model, inspired by [36, 77, 104], to identify the performance Pareto frontier and generate corresponding system schedules. This cost model is based on XPU, a generic systolic-array ML accelerator [3, 49, 104], and serve as the core engine of `RAGO` for evaluating various RAG paradigms and configurations. Below, we summarize the key contributions of our work:

- We propose `RAGSchema`, a RAG workload abstraction that simplifies RAG workload representation and enables systematic performance characterization and optimization.
- Using `RAGSchema`, we identify key system design decisions and performance trade-offs from characterizing four representative RAG paradigms and their instantiations.
- We develop `RAGO`, a systematic optimization framework that optimizes scheduling policies for efficient RAG serving. Our results show that `RAGO` delivers up to 2× improvement in QPS per chip and a 55% reduction in time-to-first-token latency compared to RAG serving systems built on LLM-only systems.

2   Background

Why RAG outshines LLM-only systems? LLM-only systems often struggle to achieve high factual accuracy or providing up-to-date information [34, 38, 51–53, 62, 63]. RAG addresses these limitations by combining the linguistic capabilities of LLMs with real-time knowledge retrieval. During offline pre-processing, external textural knowledge is encoded as vectors using an LLM and stored in a vector database. At serving time, relevant knowledge is retrieved via vector search, assessing relevance by comparing the similarity between prompt's vector representation and those in the

database. The retrieved knowledge is then appended to the prompt, refining the quality of the LLM's responses.

By virtue of this combination, RAG systems offer several key advantages over LLM-only systems. *First*, RAG systems simplify knowledge updates by allowing external databases to be modified independently [21], unlike LLMs, which require retraining or fine-tuning [21, 63]. *Second*, RAG reduces "hallucination"—a phenomenon where LLMs generate factually incorrect or entirely fictitious information. For instance, a traditional LLM might confidently assert that "Thomas Edison invented the internet", despite this being obviously false. RAG's reliance on external, up-to-date databases helps mitigate these errors by grounding the model's output in real, retrievable data [63, 67]. *Finally*, RAG systems achieve comparable or better generation quality with models that are one to two orders of magnitude smaller than LLMs [34, 38, 51–53, 62, 63]. While conventional LLMs require extensive parameters to encode a vast range of general knowledge [22, 24, 81, 89], RAG partially offloads this knowledge storage to an external database, retrieving only the most relevant content during inference.

LLM-only serving systems. Serving LLM-only systems typically involves two distinct stages: prefix (prompt computation) and decode (token generation) [78, 110]. The prefix stage processes the input prompt to generate the first output token and populate the associated key-value (KV) cache [96], which holds the encoded representation of the input context. The decode stage, on the other hand, generates subsequent tokens one at a time in an auto-regressive manner, relying on the KV cache from the prefix stage.

Modern LLM serving systems [78, 110] often disaggregate these stages, operating on separate accelerator to accommodate their distinct workload characteristics. This disaggregated design is essential for performance due to the distinct workload characteristics of the two stages [78, 110]. The prefix stage processes the entire input sequence at once, making it highly compute-intensive. Even with small batches, the prefix stage benefits from accelerators with high computational throughput to handle the full sequence length efficiently [78]. In contrast, the decode stage is memory-bound, as each inference step requires accessing the KV cache of previous tokens, while the amount of computation is small [78]. In addition to workload differences, these two phases affect different performance metrics with different SLAs: time-to-first-token (TTFT) for the prefix phase and time-per-output-token (TPOT) for the decode phase. Ultimately, optimizing the performance of LLM-only serving often depends on efficient resource allocation between the prefix and decode stages [78].

Vector search for retrieval. Another core component in RAG systems is retrieval, which identifies information from external knowledge databases. A common approach to performing this retrieval is *vector search*, which has become the cornerstone of recent information retrieval systems [39, 74]. Vector search enables the system to assess semantic relevance by encoding both documents and queries as high-dimensional vectors (e.g., hundreds to thousands dimensions), where proximity in this vector space reflects semantic similarity.

In practice, vector search retrieves the $\mathcal{K}$ most similar vectors to a given $\mathcal{D}$-dimensional query vector x from a database $\mathcal{Y}$ populated with many $\mathcal{D}$-dimensional vectors. This similarity is

typically computed using metrics such as L2 distance or cosine similarity [39, 74]. Since exact $\mathcal{K}$ Nearest Neighbor (KNN) search is costly on large-scale datasets, real-world vector search systems adopt *Approximate Nearest Neighbor* (ANN) search algorithms, which provide a scalable alternative to exact KNN by trades recall for much higher system performance.[2]

The *IVF-PQ* algorithm, which combines an inverted file (IVF) index with product quantization (PQ) [39], is one of the most widely used approaches for large-scale vector search in RAG [21, 38, 52]. IVF-PQ is frequently preferred over other ANN algorithms, such as graph-based search algorithms [29, 30, 71, 73, 74, 108, 111], due to its memory efficiency (e.g., one byte can represent 4∼16 dimensions in PQ [39, 43, 47]) —a crucial advantage when RAG systems operate on large databases, sometimes containing up to 64 billion vectors (92 TB before quantization) [21, 97].

Two popular open-source libraries for IVF-PQ are Faiss [4] and ScaNN [7, 33], exemplifying CPU-bound and memory-bound PQ variants, respectively. Faiss employs a high-precision quantization variant, resulting in a CPU-bound search process [14, 43]. In contrast, ScaNN adopts lower-precision quantization [91], achieving higher CPU throughput and shifting the workload toward being memory-bound.

3 Structuring the Complex Terrain of RAG Serving

In this section, we first describe four representative RAG paradigms with increasingly diverse and complex RAG pipelines. We then describe RAGSchema (§3.2), a structured abstraction to capture this workload diversity, serving as a foundation for serving performance characterization (§5) and optimization (§6).

3.1 Representative RAG Paradigms

We now show the workload diversity by describing the following representative RAG paradigms:

Paradigm I: Hyperscale Retrieval. Hyperscale retrieval plus smaller LLMs can be used as an alternative to larger LLMs [21, 86, 97]. Prior work has shown that RAG systems can match or even surpass the quality of LLM-only systems when database sizes are sufficiently large [21, 86]. This is achieved while using sufficiently smaller models —approximately one-tenth the parameters of their LLM-only counterparts [21, 97]. This quality parity is achieved because LLM-only models rely on their vast parameter sets to encode comprehensive knowledge during training [22, 24, 81, 89], whereas RAG systems dynamically integrate external knowledge at inference time, reducing the need for extensive parameterization within the model itself.

Paradigm II: Long-Context Sequence Processing. Another common paradigm is to use RAGs to facilitate long-context processing [56, 68, 101]. For example, when answering questions based on a lengthy document (e.g., with more than 100K tokens) that a user has uploaded, a straightforward solution is to use the entire context — similar to use cases in Gemini 1.5 [93], NotebookLM [5], and ChatGPT [6] — as a prompt. However, this approach is often prohibitively expensive due to the large number of tokens to process. Instead, an efficient alternative is to treat the user-provided long document as a

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[2]We use "vector search" and "ANN search" interchangeably.

Table 1: RAGSchema component names, descriptions, and corresponding example design parameters.

RAGSchema Components	Description	Example
Document Encoder	Model size (parameters) of the encoder used to convert database documents and queries into vector representations.	120M
Vector Dimensionality	The number of dimensions for each database vector.	768-dim
Database Vector Number	Number of the database vectors, depends on the corpus size and passage chunk lengths.	1,000
Retrieval Frequency	Whether iterative retrievals are permitted during decoding and number of retrievals per sequence.	Four per sequence
Queries Per Retrieval	Number of query vectors used per retrieval (one or multiple).	Two per retrieval
Query Rewriter	Model size of the generative query rewriter, if applied.	8B
Query Reranker	Model size of the retrieval results reranker (usually an encoder-only model), if applied.	120M
Generative LLM	Represents the model size of the main generative LLM used for answer generation.	70B

knowledge database, retrieving only the relevant information needed to answer the questions. This method substantially reduces the prompt size by avoiding the need to load the full text into the model's context window. Recent studies [56, 101] demonstrate that this retrieval-based approach achieves similar response quality to using the full document as a prompt, providing a practical balance between cost and quality in handling long contexts. In contrast to the paradigm I, RAG for long-context processing introduces two key modifications. First, this setup includes a database encoder, which is necessary for constructing the database when the long context is initially provided. Second, the database is orders of magnitude smaller. For example, given a context length of 100K tokens and a passage chunk size of 100 tokens, the database only consists of 1K vectors, compared to tens to hundreds of billions of vectors in paradigm I [21, 86].

Paradigm III: Iterative Retrievals. While a single retrieval at the beginning may suffice in some scenarios, recent studies [21, 45, 95] indicate that iterative retrievals —periodically updating retrieved content during generation— can significantly enhance model quality. Such update of the retrieved content is particularly valuable in scenarios requiring multi-hop reasoning, where each retrieval provides additional context to guide the subsequent token generation process [95, 101]. In this configuration, the decoder initiates retrievals at flexible intervals during generation. Upon issuing a retrieval, the generation of this sequence temporarily pauses the token generation, to process newly retrieved content through the prefix phase. Only after integrating this additional context does the decoder continue generating the rest of sequence.

Paradigm IV: Query Rewriter and Reranker Users often pose vague or complex queries, making it challenging to retrieve relevant information directly. To address this, the retrieval process can be significantly improved by incorporating pre-processing and post-processing steps [13, 23, 31, 72]. For pre-processing, recent studies [23, 72] demonstrate that leveraging an LLM to rewrite the user's query can improve retrieval quality. This LLM may either rephrase the query for clarity or decompose complex questions into multiple simpler queries that cover different aspects of the user's original intent [23, 72]. Once the initial results are retrieved through vector search, a reranking model can be applied as a post-processing step [1, 13, 31]. The reranker improves content retrieval quality by scoring each document's relevance beyond simple vector similarity and choosing documents that more closely align with the user's intended question.
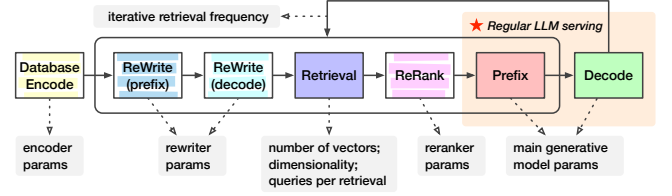
Figure 3: Describing general RAG pipelines with RAGSchema.

3.2 RAGSchema for Workload Abstraction

Given these diverse paradigms, RAG workloads exhibit significant variability across algorithm configurations in the following ways. First, retrieval configurations can vary dramatically. Database sizes may span several orders of magnitude [21, 56, 68, 86]; a retrieval may involve not a single query vector [35, 62] but multiple ones [20, 23, 98]; and some models support iterative retrievals during the generation process [21, 45, 95]. Second, a RAG system may include several models in addition to the main generative LLM. These auxiliary models include a database encoder for processing real-time uploaded documents [57, 84]; a query rewriter model [23, 72] to rephrase user queries; and a result reranker model [1, 13, 31] to score retrieved information.

To navigate the complex RAG configuration space, we introduce **RAGSchema**: *a structured and modular abstraction that captures the key performance-relevant attributes of various RAG serving workloads.* As visualized in Figure 3 and detailed in Table 1, RAGSchema defines both (1) the execution flow of the RAG pipeline and (2) the configuration of its components. For the RAG pipeline definition, optional stages[3]—such as the database encoder, query rewriter, reranker, and iterative retrieval— can be included or omitted. For each included component, RAGSchema specifies relevant configurations, including model parameter counts, vector dimensionality, number of database vectors, queries per vector, and iterative retrieval frequency if applicable.

3.3 Empirical RAG Performance Trade-off Analysis

Even though precise bottlenecks and tradeoffs depend on exact RAGSchema, high-level performance bottlenecks in RAG systems are driven by pipeline imbalance and Amdahl's law (in case of dependencies). In this section, we make general observations about RAG workloads, and quantify in §5 using detailed performance model.

We estimate RAG throughput for inference and retrieval components using FLOPS for inference and bytes accessed for retrieval. Note the

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[3]A "stage" refers to the execution of a RAG pipeline component.

precise throughput depends on system-level factors such as CPU server efficiency, XPU capability, and scheduling policies.

Inference components. For a model with size M and a sequence length L, the FLOPs required for processing the entire sequence are approximately: $\text{FLOPs}_{\text{inference}} \approx 2 \cdot M \cdot L$ for short sequences (e.g., $L \le 10^3$).

Retrieval component. The retrieval workload is represented as the number of bytes of database vectors processed per query. Unlike model inference, decoding quantized database vectors represents a fundamentally different workload where FLOPs is not an appropriate metric [14, 43]. Given a database with N_{dbvec} vectors, where each vector consists of B_{vec} bytes, and each query scans a subset of P_{scan} percent of database vectors, the total bytes to scan per query is approximately: $B_{\text{retrieval}} \approx N_{\text{dbvec}} \cdot B_{\text{vec}} \cdot \frac{P_{\text{scan}}}{100}$.

End-to-end RAG performance. While the latency of RAG serving is the sum of the latencies of each stage in the RAG pipeline, the throughput of the pipeline is determined by its slowest stage (excluding iterative retrieval paradigm for now, as it follows a different pattern discussed in §5.3). For a RAG pipeline with m stages, where each stage has a throughput denoted by QPS_i ($i=1,2,...,m$), the end-to-end RAG serving throughput is: $\text{QPS}_{\text{RAG}} = \max(\text{QPS}_1, \text{QPS}_2, ..., \text{QPS}_m)$.

From this high-level model, we can draw several key insights. First, retrieval can become a bottleneck when its workload ($N_{\text{dbvec}} \cdot B_{\text{vec}} \cdot \frac{P_{\text{scan}}}{100}$) is high while the inference workload ($2 \cdot M \cdot L$) is relatively low. Second, in paradigms with multiple inference components, any model can become critical depending on its size M and processed sequence length L, which may vary based on the model's role. Finally, the cumulative effect of multiple inference stages and retrievals can significantly impact overall serving performance. We discuss detailed evaluation methodology and quantitative characterization in the subsequent sections.

4 Methodology

This section outlines the methodology used to characterize RAG performance (§5) and evaluate RAGO across various configurations (§7).

Models and database. We evaluate four LLMs—Llama-3 1B, 8B, 70B, and 405B [26]—covering size scales comparable to those used in [64, 86, 97]. As RAG quality continues to benefit from larger knowledge corpora [21, 86], we adopt a hyperscale database [21]. This database contains 64 billion passages, each encoded as a 768-dimensional vector [21], making it approximately 400× larger than the largest academic vector search datasets [9, 16, 88]. We apply product quantization (PQ) as in [21] to compress each vector to 96 bytes (1 byte per 8 dimensions), resulting in a 5.6 TiB quantized vector database. Following the index recommendations of the ScaNN library [7], we use a balanced fanout of 4K vectors per node across the three-level tree index [90] ($(64 \times 10^9)^{1/3} = 4 \times 10^3$). To balance retrieval quality and performance, each query is compared against 0.1% of the database vectors by default, as this setup has shown high recall (over 90%) in billion-scale datasets [43].

LLM sequence lengths. In line with common RAG use cases such as question-answering [23, 62, 95], we evaluate sequence lengths

Table 2: Performance specifications of three versions of XPUs. We report performance on XPU-C ($\star$) by default.

	XPU-A	XPU-B	$\star$ XPU-C
TFLOPS	197	275	459
HBM (GB)	16	32	96
Mem. BW (GB/s)	819	1200	2765
Inter-Chip Link BW (GB/s)	200	300	600
Resembles	TPU v5e [11]	TPU v4 [10]	TPU v5p [12]

derived from QA datasets [17, 48, 83], where the question lengths range from six to 42 tokens. To simplify the search space, we use 32 tokens as the typical question length. The input prompt length includes both the question and relevant retrieved content. The typical nearest neighbor retrieved ranges from two to 10 [15, 21, 45, 95], each with an average length of 100 tokens. We pick five as a common value for our evaluations. Given this, we approximate the average length of input prompt (question + relevant retrieved contents) to 512 tokens. For generation lengths (decode stage), we rely on data from long-form QA [28] and chatbot datasets [8, 54], selecting 256 tokens as a representative decode length.

System setup. Our evaluation assumes a data center model-serving environment with abundant resources to support various system configurations. Across the RAG serving stages (e.g., prefix, decode), we allocate a total of 16 to 32 servers hosting 64 to 128 XPUs (4 XPUs per server), as a minimum of 16 servers is required to ensure sufficient host memory capacity for the dataset (5.6 TiB after quantization). An XPU refers to a generic systolic-array-based ML accelerator [3, 49]. The number of XPUs allocated to each model component is configured in powers-of-two scaling factors (e.g., 1, 2, 4, etc.). Each XPU, inspired by the setup of TPU v5p accelerators [12], is equipped with 96 GB of high-bandwidth memory (2.7 TB/s) and 459 TFLOPS of compute capacity. The XPUs are interconnected via a high-bandwidth 3D torus topology, offering 600 GB/s of inter-chip bandwidth (six 100 GB/s links per chip). We also evaluate two other versions of XPUs, as shown in Table 2, for ablation studies. The host CPUs are modeled after AMD EPYC Milan processors, featuring 96 cores, 384 GB of memory, and 460 GB/s of memory bandwidth. We assume that XPU host servers support distributed retrieval across large databases.

Simulation setup. RAG performance is reported by assembling the costs of all model inference and retrieval stages, based on a search across various system configurations (details described in §6). We now describe the production-grade simulators used to measure inference and retrieval performance.

(a) Inference performance modeling. We adopt an in-house calibrated XPU simulator for inference simulation. The simulator is well-correlated with the production-grade XPU accelerators across a set of real-world ML models. The simulator abstracts inference as a sequence of operators, where total latency is computed as the sum of each operator's execution time and the associated data movement costs, similar to other established ML simulators [77, 104]. The cost of each operator is calculated using a roofline model that accounts for compute, memory, and network costs. For multi-XPU inference, the simulator explores variousevaluates a range of model sharding

Table 3: RAGSchema of the workloads used in case studies.

RAGSchema Components	Case 1	Case 2	Case 3	Case 4
Document Encoder	N/A	120M (768-d)	N/A	N/A
Database Vector Number	64B	1/10/100K	64B	64B
Retrieval Frequency	1	1	2/4/8	1
Queries Per Retrieval	1/2/4/8	1	1	1
Query Rewriter	N/A	N/A	N/A	8B
Query Reranker	N/A	N/A	N/A	120M
Generative LLM	1/8/70/405B	8/70B	8/70B	8/70B

strategies, including tensor parallelism [82, 87], pipeline parallelism [37, 76], or the hybrid approach. Each accelerator is assigned a subset of inference components, with inter-machine communication costs explicitly modeled to ensure realistic latency estimations.

(b) Retrieval performance modeling. Our retrieval simulation is based on ScaNN [7, 33], a product quantization library (§ 2) that demonstrates state-of-the-art performance across dozens of algorithms in the ANN benchmark [2]. We implement the ScaNN performance model described in [90], which models the search process as a sequence of vector scan operations at each level of a multi-level tree [7, 90]. The total retrieval latency is calculated as the sum of the latencies for these scan operations. ScaNN dedicates one thread per query and parallelizes batches of queries across multiple threads. The cost of each operator is calculated by a roofline model that factors in batch sizes, the number of CPU cores, per-core CPU processing throughput, and memory bandwidth. For large databases requiring distributed search across multiple servers, we assume each server holds a shard of the dataset with independent indexes. Queries are routed to all servers, and results are aggregated. The workload is balanced across servers, with negligible overhead for broadcast and gather operations. To populate simulator parameters, we benchmark the maximum achievable per-core throughput and memory bandwidth by running open-source ScaNN [7] on smaller datasets configured with the same tree node sizes (4K vectors per node) as the 64-billion vector database. On AMD EPYC 7R13 CPUs with 24 cores, ScaNN achieved a PQ code scanning throughput of 18 GB/s per CPU core, with approximately 80% memory bandwidth utilization. We then calibrate the retrieval performance model using internal production datasets comparable in scale to the 64-billion vector dataset used in our study (§4).

Performance metrics. We report common metrics used in the evaluation of LLM systems [78, 110]:

- [**TTFT**] **Time-to-First-Token** ↦ average latency from request reception to the generation of the first output token.
- [**TPOT**] **Time-Per-Output-Token** ↦ average latency between generating each output token in a sequence.
- [**QPS**] **Queries-Per-Second** ↦ maximum throughput, or the number of requests the system can process per second.
- [**QPS/Chip**] **Queries-Per-Second/Chip** ↦ QPS normalized by chip count, reflecting system cost efficiency.

Since continuous batching [54, 100] is enabled in the decode stage, we report the worst-case TPOT latency. This is because sequences in the batch can be at different stages of generation — some generating the first token and others generating the last ones — and performance is determined by the latter. In contrast, prefix operates deterministically, allowing us to report the precise TTFT latency.
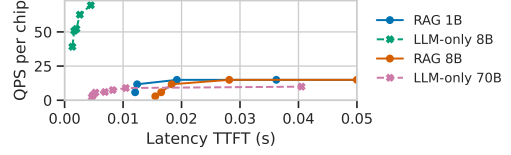
Figure 4: Larger LLM versus RAG with smaller models.

5 RAG Serving Performance Characterization

In this section, we characterize workloads using four case studies, each representing a RAGSchema instantiation of a distinct RAG paradigm described in §3.1. These case studies highlight the performance variability across RAG workloads, quantify the impact of paradigm choices on system performance, and motivate the need for our RAG optimization framework (§6).

Characterization methodology. We evaluate performance using the methodology outlined in §4. Unless otherwise specified, the end-to-end performance plots depict the performance Pareto across all system scheduling options. The time breakdown assume (a) four XPUs per host server and (b) each component operating at its maximum QPS/Chip. The evaluated workloads are summarized in Table 3. While all configurations in the table are analyzed, the plots highlight a representative subset to avoid redundancy when similar trends are observed across multiple configurations (e.g., model sizes).

5.1 Case I: Hyperscale Retrieval

We adopt configurations similar to those in RETRO [21], replicating its database setup and similar sized LLMs along with more recent, larger models. The RAG system performs only *one* retrieval at the beginning, which may involve one or multiple query vectors, as suggested by recent studies [20, 23, 98].

Takeaways: Hyperscale retrieval can pose a significant bottleneck in RAG pipelines. This bottleneck becomes increasingly dominant with (1) smaller LLM, (2) multi-query retrievals, (3) better inference accelerators, (4) shorter prefix and decode sequence lengths, and (5) higher retrieval quality.

System performance comparison (RAG vs. LLM-only). Figure 4 compares RAG and LLM-only systems across different model sizes, with TTFT latency on the x-axis and QPS/Chip on the y-axis. As shown in the RETRO paper [21], RAG can achieve similar or superior generation quality to LLM-only systems with an order of magnitude fewer parameters. Here, we extend this comparison to system performance. Our results indicate that RAG 8B outperforms LLM-only 70B in QPS/Chip by a factor of 1.8×, though this advantage is tempered by the retrieval overhead and the longer prompts required to incorporate retrieved information (thus only 3.2× FLOPs reduction for inference). Consequently, the QPS/Chip gain is not directly proportional to the reduction in parameter size. Interestingly, the results suggest that RAG model sizes can be increased up to a certain limit without compromising QPS/Chip, as retrieval performance is the limiting factor. For example, RAG 1B and RAG 8B exhibit similar QPS, highlighting the importance of system performance analysis in determining how much larger RAG
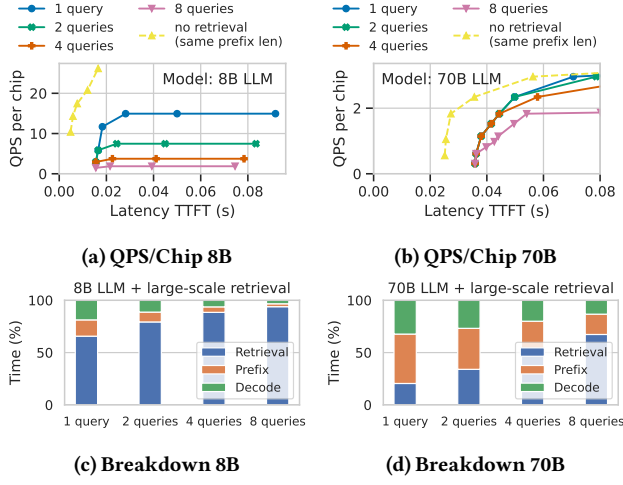
(a) QPS/Chip 8B

(b) QPS/Chip 70B

(c) Breakdown 8B

(d) Breakdown 70B

Figure 5: RAG performance given various model size and query numbers for hyperscale retrieval.

(a) XPU Gen

(b) Retrieval Config

(c) Seq. Length

Figure 6: The percentage of retrieval time across hardware, retrieval configurations, and sequence lengths in Case I.

(a) QPS/Chip 70B

(b) Breakdown 70B

Figure 7: RAG performance for long-context processing.

models can scale. While RAG models offer significant advantages at certain scales, their benefits may diminish at lower parameter counts as retrieval latency becomes a bottleneck. For example, despite RAG 1B having only one-eighth the parameters of LLM-only 8B, its QPS/Chip does not scale proportionally, because the retrieval overhead in RAG outweigh the benefits of reduced model size.

Sensitivity to model size. Figure 5a and Figure 5b present the QPS/Chip for the 8B (left) and 70B (right) models, alongside time breakdowns for retrieval, prefix, and decode stages in Figure 5c and Figure 5d. The yellow line represents a "no retrieval" configuration, where retrieval is omitted while the prefix remains the same length. For the 8B model, retrieval is the primary bottleneck; as query counts double, QPS nearly halves due to increased retrieval demands. Conversely, for the 70B model, inference initially limits performance until four queries per retrieval. At higher query vector counts per retrieval (e.g., 8 queries), the bottleneck shifts, and retrieval starts to dominate, as seen in the time breakdown in Figure 5d.

Sensitivity to XPU versions. Figure 6a shows the impact of XPU capability on the percentage of time spent on retrieval for LLMs ranging from 1B to 405B parameters. As the XPU capabilities advance (from version A to C), the proportion of time spent on retrieval increases by up to 25%. While for larger models (e.g. 405B), LLM remains the dominant bottleneck in RAG serving, retrieval is dominant factor for RAG with small models (50% - 75% across XPUs versions). Overall, with more advanced ML accelerators, system efficiency increasingly depends on optimizing retrieval processes.

Sensitivity to sequence lengths. Figure 6c illustrates the sensitivity of retrieval overhead to changes in decode length and prefix length given for 8B model. The retrieval overhead varies significantly with both decode and prefix lengths — retrieval bottlenecks diminish as sequence lengths increase, shifting retrieval from a primary bottleneck to a secondary factor. For example, 86.3% of the time is spent on retrieval at shorter sequence lengths (e.g., 128
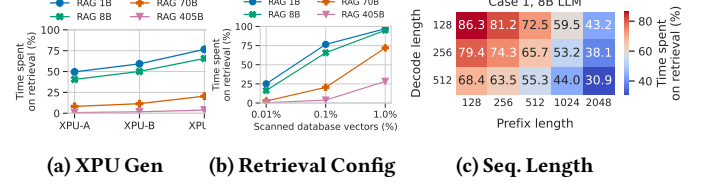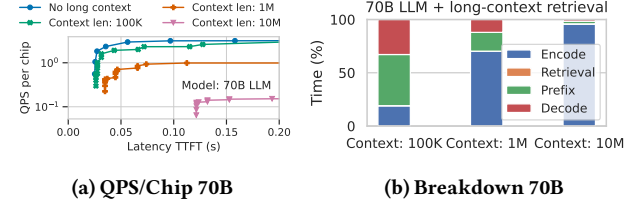
or 256), while the retrieval overhead drops to just 30.9% with longer prefix and decode lengths (2048 and 512). Adjusting the prefix and decode lengths results in unequal changes in the percentage of retrieval time. For example, in a setting of 128 tokens for both prefix and decode, increasing the prefix length to 256 tokens reduces retrieval time from 86.3% to 81.2%, while increasing the decode length to 256 tokens lowers it to 79.4%. This difference occurs because prefix inference is inherently faster than decoding the same number of tokens due to the autoregressive nature of decoding.

Sensitivity to retrieval configurations. Retrieval performance in RAG workflow is highly sensitive to the percentage of database vectors scanned per search. Regardless of the ANN algorithm used, ANN search does not conform to a fixed workload — there is an fundamental trade-off between retrieval performance and quality: scanning more vectors improves quality but reduces performance [39, 74]. This trade-off is further influenced by data distribution; for instance, with the same algorithm, hardware, and QPS, one dataset may achieve over 90% recall, while another may fall below 50% [88]. While prior evidence suggests that higher recall can enhance generation quality [44, 61], there has been no consensus on the optimal recall threshold. Figure 6b illustrates the impact of varying the percentage of scanned database vectors, ranging from 0.01% to 1% (with 0.1% as the default), on the proportion of time spent on retrieval across different model sizes. For all models, increasing the scanned database vectors significantly amplifies the proportion of time spent on retrieval, highlighting the substantial variability in retrieval performance across RAG configurations.

5.2 Case II: Long-Context Sequence Processing

As shown in Table 3, we evaluate context lengths ranging from 100K to 10M tokens, resulting in a database of 1K to 100K vectors, with each chunk sized at 128 tokens and small overlaps between chunks. We use a sentence transformer model with 120 M parameters [84] to encode the passages, generating 768-dimensional embeddings, as relatively
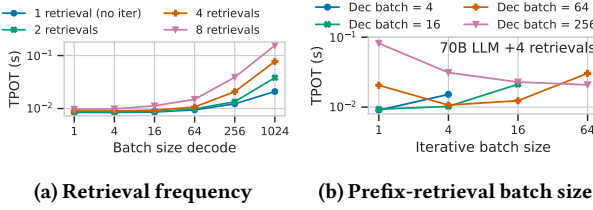
(a) Retrieval frequency		(b) Prefix-retrieval batch size

Figure 8: RAG performance with iterative retrievals.

compact models are sufficient to achieve high retrieval quality [84]. Instead of ANN search, we use brute-force kNN search due to the high indexing costs associated with newly generated embeddings.

Takeaways: In contrast to the Case I, retrieval performance plays a minimal role here. Instead, the database vector encoding process emerges as the bottleneck, even with a small encoder model, due to the significantly longer context the encoder must process compared to the generative LLM.

RAG vs. long-context LLMs. Despite the high encoding cost, RAG is significantly more efficient than processing the entire long context as a prompt (long-context LLM). For instance, with a 1M-token context and a 70B LLM, RAG reduces the required prefix length to 512 tokens, achieving a speedup of 2852.6× in TTFT and 6633.9× in QPS/Chip. This is even considering an efficient long-context LLM applying global attention to all tokens in only one out of every four layers, while the rest layers only apply local attention to the last 128 tokens. This cost efficiency arises for two primary reasons: (I) In long-context RAG, the database encoder, typically a small model (e.g., 120M parameters), performs the encoding. This is much less computationally intensive compared to the LLM-only system with billions of parameters, which would require significantly more FLOPs if fed the entire context. (II) Long-context LLMs require key-value caches for every token, consuming substantial XPU memory (i.e. cost). In contrast, RAG significantly reduces prompt lengths, saving XPU memory. This distinction enables RAG to handle larger batch sizes during generation, increasing QPS/Chip.

Sensitivity to context length. Figure 7 presents performance trends when the input context length scales from 100K to 10M tokens for the 70B model. "No long context" line represents the standard prompt length of a 512-token prefix. As the context length increases, RAG performance gradually degrades due to the increasing cost of context encoding, even though retrieval enables prompt truncation for the generative LLM. This happens due to database encoding becoming the bottleneck (Figure 7), especially at longer context lengths (>1M). Notably, encoding time scales with context length, despite the relatively small encoder applied (120M parameters), due to the sheer volume of data processed. Therefore, caching the generated embedding for potential reuse can significantly reduce computation with minimal cost. For instance, caching 10K 768-d database vectors in FP16 format (for 1M tokens) requires only 15 MB of CPU memory or storage. The retrieval time is minimal even when using brute-force search due to small database (1K-100K vectors vs 64B in other cases).

5.3 Case III: Iterative Retrievals + Prefix

The iterative retrieval setup allows for 2, 4, or 8 retrievals per sequence generation process. Each retrieval is triggered at random intervals during the 256-token decoding process, with retrievals uniformly distributed across token positions.

Takeaways: Batch sizes for iterative retrievals must be carefully selected, as they significantly impact TPOT latency. Larger batch sizes improve retrieval and prefix throughput but may stall decoding, negating the gains.

Sensitivity to retrieval frequency. Figure 8a examines the impact of different retrieval frequencies (1-8 per sequence) on TPOT latency as the decode batch size increases from 1 to 1024, as QPS/Chip shows similar trends as multi-query retrieval in Case I. The results indicate that TPOT latency increases with both retrieval frequency and the decode batch size. At smaller decode batch sizes (one, four, and 16), the TPOT latency differences between retrieval frequencies are relatively minor. This is because, at these lower batch sizes, the decode step remains the dominant factor in TPOT latency, contributing approximately 60%-80% of the latency, while the effect of additional retrievals remains limited. At higher batch sizes, however, the decode process achieves higher QPS/Chip, reducing its share of the overall TPOT latency. This shift in bottleneck exposes the impact of retrieval frequency, as retrievals become the primary contributor to latency. Consequently, at larger batch sizes, the latency gap across different retrieval frequencies widens, making the increased time required for multiple retrievals more pronounced.

Sensitivity to iterative retrieval batch size. In Figure 8b, we observe the nuanced interplay between decode batch size, iterative retrieval-prefix batch size and TPOT latency for a 70B model processing four retrievals per sequence. At smaller decoding batch sizes (4 and 16), increasing the iterative retrieval batch size results in a noticeable increase in latency. This is due to the inherent challenge in finding enough retrieval requests to batch within an active set of decoding sequences over a given time interval, introducing stalls. For decode batch sizes of 256, the relationship reverses. As the iterative retrieval batch size increases, latency decreases. Here, the abundance of active decode sequences allow the system to batch retrieval requests more rapidly, enabling improved performance. The decode batch size of 64 presents a particularly intriguing case: it reaches its lowest TPOT at retrieval batch size of four. This optimal point represents a balance where idle time is minimized and the batching of retrieval requests is most efficient. However, beyond this threshold, latency begins to climb again as it becomes progressively harder to amass a sufficient number of retrieval requests for efficient batching. This behavior illustrates the delicate balance in RAG system performance when trying to balance retrieval performance and decoding efficiency.

Figure 9 further illustrates the phenomenon of decoding slowdown caused by idleness. Figure 9a visualizes the batching process, while the heatmap (Figure 9b) shows normalized decoding latency (compared to no retrieval) as a function of the decode batch size (x-axis) and iterative retrieval batch size (y-axis). In this evaluation, the retrieval and prefix stages are assumed to have zero latency, isolating the slowdown to the batching-induced waiting time. The results show that the effective latency is highly sensitive to the ratio
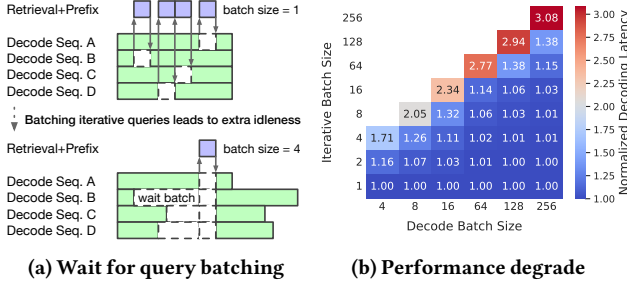
(a) Wait for query batching   **(b) Performance degrade**

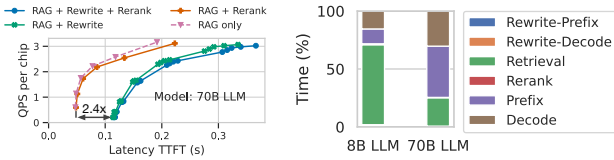**Figure 9: Decode idleness due to batched iterative queries.**

Figure 10: RAG performance with rewriter and reranker.

of decode batch size to iterative retrieval batch size. When these batch sizes are similar (e.g., both set to 64), the normalized decoding latency reaches up to 2.78. This increase occurs because one of the requests may generate a larger number of tokens before the next retrieval, resulting in idleness becomes a dominant factor. For smaller ratios (e.g., decode batch size 64 and retrieval batch size up to 16), latency increases more gradually, indicating a more balanced workload with minimal idleness. This observation aligns with Figure 8b, where, for a decode batch size of 64, increasing the iterative retrieval batch size from 16 (1.14 normalized latency due to idleness) to 64 (2.78 normalized latency due to idleness) causes a significant increase in TPOT latency. In summary, the results suggest that (a) when there is a large pool of XPUs that allows for large decoding batches, one can choose the iterative batch size that saturates database throughput, however, (b) with a smaller pool of XPUs and smaller decoding batch sizes, the optimal decoding batch size may actually be lower than the one that fully saturates the database.

5.4 Case IV: Query Rewriter and reranker

In this setup, we extend Case I by integrating an 8B query rewriter model [26] and a 120M reranker [84].

Takeaways: While the reranker has negligible impact on overall RAG performance, the query rewriter can significantly increase TTFT latency due to its autoregressive nature.

System performance comparison (RAG vs RAG with rewrite and rerank). Figure 10 (left) presents the performance of various RAG configurations with or without rewriter and reranker. The results indicate that QPS/Chip remains largely unaffected by the addition of the rewriting and reranking modules. This is further validated from Figure 10 which shows that negligible time is spent in rewriter and reranker stages. However, the TTFT latency increases significantly (2.4×) when the rewriter is included, due to its autoregressive generation nature, while reranking has minimal
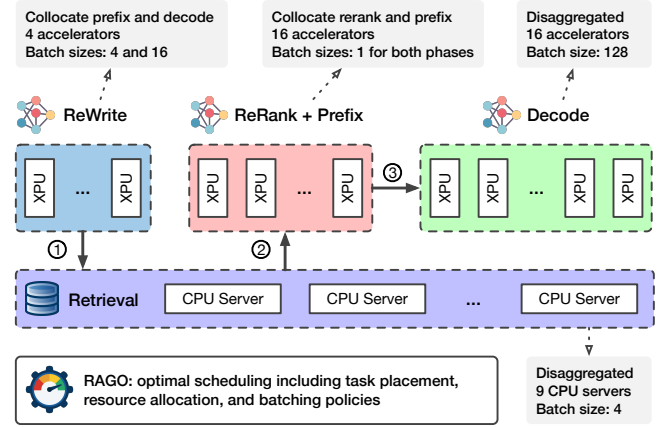
impact on TTFT. This highlights the importance of considering an application's latency tolerance when integrating the rewriter component, as it can substantially affect the user experience in latency-sensitive scenarios.

6   RAGO: Systematic RAG Serving Optimization

Given the heterogeneous components and high workload variance across RAG (§5), one-size-fits-all systems are inherently inadequate for achieving optimal serving efficiency. To overcome this challenge, we introduce RAGO, a systematic framework to design and optimize RAG serving systems across diverse configurations. RAGO determines an optimized scheduling policy tailored to a specific RAGSchema and a defined performance target. The following sections expound on the components of RAGO and its overall design.

6.1   RAGO Scheduling Decisions

Each scheduling solution comprises three pivotal system decisions: *task placement, resource allocation, and batching policy.* Figure 11 illustrates an example how these decisions come together to optimize a RAG serving pipeline under the constraint of 36 XPUs. In this example, RAGO adopts a hybrid collocation-disaggregation task placement strategy. Specifically, the pipeline is organized into two collocated subsystems: (1) the rewrite-prefix and rewrite-decode phases; and (2) the rerank and prefix phases of response generation. This organization ensures that tightly coupled tasks are efficiently grouped. Resource allocation is tailored to the computational demands of each subsystem. For instance, the query rewriter is assigned four XPUs, while the decoding phase, requiring significantly higher computational power, is allocated 16 XPUs. To further enhance efficiency, RAGO assigns batching policies customized to the characteristics of each phase. For example, the rerank and prefix phases prioritize low-latency processing with a batch size of one, whereas the decoding phase operates with a much larger batch size of 128 to maximize throughput. By orchestrating these decisions, RAGO acts as the engine driving optimized serving performance across diverse RAG configurations. Below, we formally describe each system scheduling decision, deferring how to search for optimal schedules to §6.2.
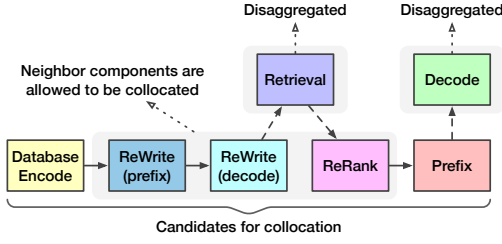

Figure 11: An example of RAGO optimizing placement, allocation, and batching policies for efficient RAG serving.

Figure 12: **RAGO** allows collocation of neighbor models.

Figure 13: Execution order of batched requests until prefix.

[I] Task placement. Recent LLM serving systems [78, 110] advocate for disaggregating the prefix and decode phases (§2), as these phases exhibit distinct workload characteristics —compute-bound vs. memory-bound— and impact TTFT versus TPOT. However, given the multiple components in a RAG pipeline (Figure 3), a natural question arises: *should RAG systems adhere to the convention of fully disaggregated designs common in LLM-only systems?* While prefix-decode disaggregation often proves beneficial (§ 2), RAG pipelines may benefit more from adopting a collocation or hybrid collocation-disaggregation strategy, particularly for components leading up to the prefix phase. First, several components in the pipeline — such as the database encoder, reranker, and the prefix phases of both the query rewriter and the main LLM — share a similar profile of high computational intensity, and thus time-multiplexing these components on the same set of XPUs can inherently mitigate workload imbalances among them. Second, components up to the prefix phase directly influence TTFT latency: while a fully disaggregated design, constrained by limited accelerator resources per stage, can prolong TTFT, collocation mitigates this by allowing all components to share the available resources, thereby reducing latency.

That said, the decision between collocation and disaggregation depends on the specific characteristics of the RAG pipeline. For instance, the decoding phase of the query rewriter is autoregressive, and scales pooly with small batch sizes even with additional XPUs [54, 100]. Thus, collocating it with the prefix phase across many chips risks underutilizing hardware resources, as analyzed in §7. To address these challenges, RAGO supports hybrid collocation-disaggregation task placement policies. This approach balances flexibility and performance, as outlined as follow. Firstly, the main LLM's prefix and decode phases remain disaggregated, consistent with the strategies in [78, 110]; Secondly, retrieval is always treated as a disaggregated task, as it operates on CPUs rather than XPUs. Finally, neighboring phases up to the prefix can be collocated (Figure 12). Collocation is restricted to consecutive neighbors to avoid excessively complicating the search space.

[II] Resource allocation. After determining task placement, RAGO assigns resources to each pipeline phase based on its computational and memory requirements. For collocated inference phases, this involves selecting the appropriate number of accelerators to ensure efficient execution. Similarly, for retrieval operations, RAGO determines the number of CPU servers required to meet workload demands. The framework balances throughput requirements and latency constraints to ensure optimal performance. Additionally, RAGO ensures that each component has sufficient accelerator or CPU
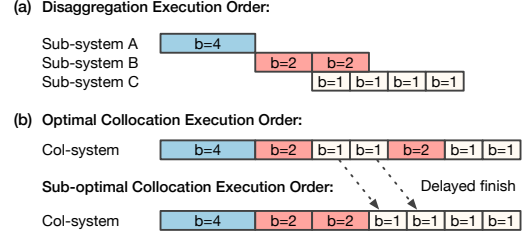
memory capacity to store the required models or database segments while meeting the specified performance targets.

[III] Batching policy. Given a batch of incoming requests, RAGO enables each stage of the pipeline to adopt varying batch sizes, offering flexibility to balance latency and throughput at each stage. For the decode stage, RAGO leverage continuous batching [54, 100] to use larger batch sizes than individual requests, thereby improving throughput, as we evaluate in § 7. Moreover, in the case of iterative retrievals (§ 5.3), RAGO allows distinct batch sizes for the *initial* retrieval/prefix pair and the *subsequent* decoder-initiated retrieval/prefix iterations. This differentiation is crucial because the initial retrieval and prefix phases directly affect TTFT, while the iterative ones primarily impact TPOT during token generation (see § 5.3).

Once batch sizes are determined, RAGO organizes their execution order to maximize efficiency based on the task placement strategy. Here, we discuss the order of stages up to prefix, as the generative LLM decode always apply continuous batching [54, 100]. In a fully disaggregated design (Figure 13(a)), execution is straightforward. As soon as (1) sufficient inputs arrive for a subsystem and (2) the subsystem completes its previous batch, it processes the new batch and forwards the output to the next subsystem. On the other hand, Figure 13(b) shows the execution order of the collocated design. For simplicity, we use time-multiplexing strategy and leave more complex strategies such as simultaneous execution as future work. In time-multiplexed designs, the throughput of the collocated system is fixed once batch sizes are set for each stage. In such cases, a stage begins execution as soon as it accumulates enough inputs. As illustrated in Figure 13, the optimal execution order prioritizes completing the final stage (b=1) early over processing another round of the second stage (b=2), thereby minimizing the average completion time of the final stage. If a retrieval operation is required between collocated stages (e.g., between the rewrite and prefix stages), the system pauses until the retrieval phase is complete before resuming the next collocated model inference phase. By optimizing batching policies and execution order, RAGO ensures that the trade-offs between latency and throughput are carefully managed for each stage, enabling efficient end-to-end RAG serving.

6.2 Searching for Optimal Scheduling Policies

Given a RAGSchema and hardware resource constraints, RAGO performs an exhaustive search across potentially millions of schedules to identify Pareto frontier for key performance metrics. Given m model inference stages, the size of the search space can be expressed as $C \cdot R^m \cdot T^m$, where C represents the number of collocation options,

R denotes the number of resource allocation options per stage, and T is the batching options per stage. RAGO operates in three main steps. First, it performs performance profiling by evaluating each RAG component individually (e.g., retrieval, prefix, etc.) under varying resource allocations and batch sizes. This evaluation relies on the calibrated analytical model introduced in §4. Next, it proceeds to schedule generation, where it explores *all* possible RAG schedules by considering (a) collocation strategies, (b) resource allocation strategies within the overall resource budget, and (c) batching strategies for each component. Finally, RAGO calculates the end-to-end performance for each schedule and identifying the Pareto frontier along with the corresponding schedule configurations.

RAGO relies on several simplification assumptions to calculate the end-to-end performance. Data movement is assumed to be negligible, as transferring retrieved tokens to accelerators requires minimal bandwidth. For instance, a 1K-token prompt involves only a few kilobytes of data movement, which incurs a latency in the range of microseconds —negligible compared to the milliseconds required to decode a single token in the RAG pipeline. Additionally, key-value (KV) cache movement between prefix and decode accelerators can be performed layer-by-layer [78], allowing it to overlap with computation, thanks to high inter-chip interconnect bandwidth (i.e., 600 GB/s, see Table 2). We follow the same methodology described in § 4 to compute decode latency per step (i.e., constant latency of the final token [100]). Finally, we simplify granularity by searching hardware resource quantities and batch sizes in powers of two.

RAGO allows users to constrain the search space to reduce search time by specifying batch size ranges and setting overall and per-stage resource constraints. For example, in the RAG paradigm I, which involves three stages and up to 128 chips, the search process takes approximately one minute. Adding an encode stage in the RAG paradigm II increases the complexity, resulting in a search time of about ten minutes, which still remains computationally tractable. For the most complex case (RAG paradigm IV), which includes six stages, the search time is kept under an hour by limiting the resource allocation options. For instance, we first fix the number of XPUs for the main generative LLM's prefix and decode stages, as they are the primary bottlenecks (Section 5.4), and only explore resource allocation options for the remaining stages (rewrite-prefix, rewrite-decode, and rerank). We leave search space pruning optimizations as future work.

7 Evaluation

We evaluate the effectiveness of RAGO by revisiting the four RAG case studies in §5. We begin with an analysis of the performance overview across all scheduling policies, followed by a detailed examination of each scheduling decision: placement, allocation, and batching.

Evaluation methodology. For evaluating placement and resource allocation decisions, we focus on case study II (C-II) —long-context sequence— and case study IV (C-IV) —RAG with rewriter and reranker. We select these case studies because of their additional components, which visibly distinguish them from LLM-only systems and introduce unique optimization challenges. For micro-batching policy evaluations under bursts of user requests, we include case study I (C-I) with hyperscale retrieval, alongside C-II and C-IV. We

exclude case study III (C-III), which focuses on iterative retrievals during decoding, as it was evaluated in details in §5.3.

7.1 Overall Performance

Baseline system. Our baseline is an extension of LLM-only systems, where additional RAG components are collocated with the prefix system of the generative LLM. Rather than arbitrarily assigning chips to prefix and decode, we carefully tune the ratio based on their time consumption. In this tuned baseline, the prefix and decode stages are allocated in a 1:1 chip ratio, reflecting their similar time requirements in the pipeline (1.2~1.4:1 across the 8B and 70B models).
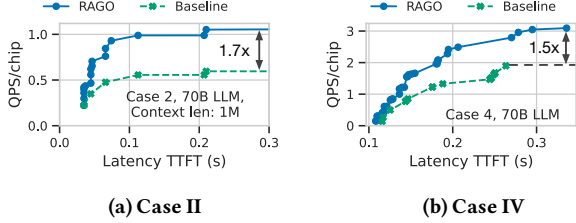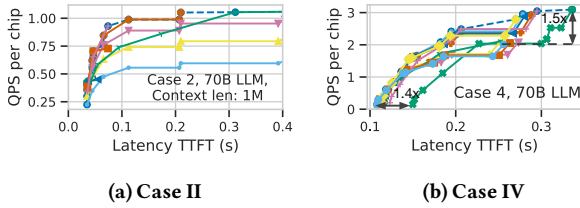
Impact of scheduling policies on QPS/Chip. Figure 14a illustrates the Pareto performance comparison between RAGO and the baseline in terms of QPS/Chip across two distinct RAG case studies. In C-II, RAGO achieves a 1.7× improvement in maximum QPS/Chip over the baseline. This speedup underscores the inefficiencies of the baseline approach, particularly in handling the encoding stage for long-context sequences. The encoder, while smaller than the generative LLM, becomes a critical bottleneck as context lengths grow. Specifically, in the baseline configuration, encoding is collocated with the prefix stage, leading to resource imbalance: decoding XPUs (50% of all XPUs) remain idle, while encode-prefix XPUs are overloaded. This imbalance can theoretically reduce QPS/Chip by up to 2.0× in the baseline, which aligns with our observed reduction of 1.94× for a large 10M-token context, though this specific data point is not plotted. On the other hand, RAGO achieves high QPS/Chip by allocating 64 out of the 96 XPUs to encoding (Table 4), reflecting the high time consumption of this stage.

A similar inefficiency of the baseline is observed in C-IV (Figure 14b), where the rewriter and reranker models, despite their relatively small size (8B and 120M), significantly impact throughput in the baseline system. This QPS drop can be attributed to two primary factors. First, collocating rewriter-decode stage and the prefix stage of the main generative LLM leads to XPU under-utilization due to the low computational intensity of the autoregressive decoding stage, particularly when handling small batch sizes. Second, retrieval operations are introduced between the rewriting and prefix stages add wait times for retrieval results (e.g., 10 ms with a batch size of one given 32 host servers), further reducing throughput. In contrast, RAGO demonstrates its ability to mitigate these bottlenecks through optimized task placement, resource allocation, and batching strategies. These results highlight the importance of disaggregating smaller pipeline stages and balancing resource distribution to unlock the full throughput potential of RAG systems.

Pareto composition analysis. Figure 15a and Figure 15b reveal how diverse placement and allocation plans contribute to the overall Pareto frontier. The dashed lines represent the global Pareto frontier, while each solid line corresponds to the Pareto frontier of a specific combination of placement and allocation strategies, with each point on a line representing a batching policy. The overall Pareto frontier is constructed from multiple distinct plans, each embodying a unique trade-off between TTFT and QPS/Chip.This diversity underscores the importance of tailoring placement and allocation strategies to the specific performance priorities of a deployment. For instance,

Table 4: Comparison of `RAGO` and baseline system schedules (placement, allocation, and batching strategies) in Case II.

Schedules	Performance		Batch Sizes				Num XPUs			
	TTFT (s)	QPS/Chip	Encode	Retrieval	Prefix	Decode	Encode	Prefix	Decode	Total
RAGO (Max QPS/Chip)	2.47	1.08	2	2	128	1024	64	16	16	96
RAGO (Min TTFT)	0.03	0.22	1	1	1	128	64 (col)	64 (col)	64	128
Baseline (Max QPS/Chip)	1.54	0.65	2	2	128	256	64 (col)	64 (col)	64	128
Baseline (Min TTFT)	0.03	0.22	1	1	1	128	64 (col)	64 (col)	64	128

(a) Case II   **(b) Case IV**

Figure 14: `RAGO` versus LLM-only system extension.

(a) Case II   **(b) Case IV**

Figure 16: Comparison of task placement plans.

(a) Case II   **(b) Case IV**

Figure 15: Performance Pareto across multiple placement and allocation plans in case 2 and 4.

(a) Collocated   **(b) Disaggregated**

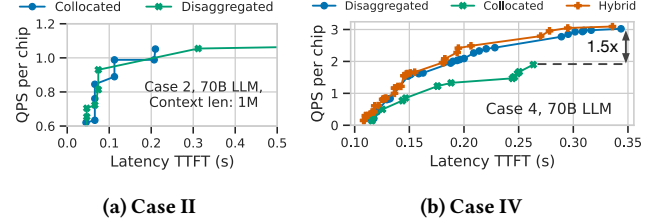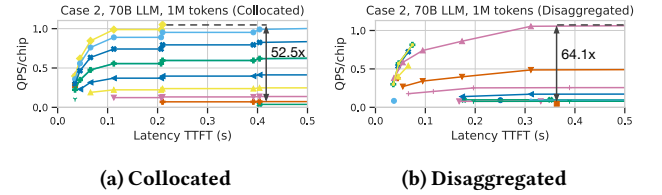**Figure 17: Comparison of resource allocation plans (case II).**

as shown in Figure 15b, selecting the most throughput-optimized plan results in a trade-off, with TTFT approximately 40% higher compared to the most latency-optimized plan, while achieving 1.5× QPS/Chip. This is because the throughput-optimized plan allocates only one chip to the query rewriter, given its minimal contribution to the end-to-end generation latency, as analyzed in §5.4. In contrast, the latency-optimized plan allocates 32 chips to the query rewriter, resulting in low resource utilization since a significant number of chips are assigned to this non-bottleneck stage. These findings emphasize that there is no one-size-fits-all strategy. Instead, the optimal placement and allocation plans must be aligned with the operational objectives, whether minimizing latency, maximizing throughput, or achieving a balance between the two.

7.2 Scheduling Policy Sensitivity Analysis

We now delve into a detailed analysis of the performance implication of each scheduling decision.

Task placement sensitivity. Figure 16 compares the impact of different task placement policies on system performance across C-II and C-IV. Each line in Figure 16a and Figure 16b represents the Pareto frontier for a specific placement strategy, illustrating the relationship between QPS/Chip and TTFT latency under these policies.

In C-II (Figure 16a), task placement sensitivity is minimal. Both collocated and disaggregated strategies yield comparable performance, as the encoder and prefix stages are computationally intensive.

Whether these stages are time-multiplexed (collocated) or spatially multiplexed (disaggregated), performance remains consistent (only 2% difference in max QPS/Chip) as long as the accelerator ratio between stages is appropriately chosen. This demonstrates that task placement decisions in this case have little effect on system efficiency, provided resources are balanced effectively.

In contrast, C-IV (Figure 16b) shows a more pronounced sensitivity to placement policies. Here, a hybrid placement strategy —combining elements of disaggregation and collocation— slightly outperforms the fully disaggregated approach and significantly surpasses the collocated plan, achieving up to a 1.5× improvement in QPS/Chip. The key advantage of the hybrid and disaggregated strategies lies in their ability to mitigate the underutilization of prefix chips, which occurs when the rewriter model is collocated with the prefix stage. By separating the rewriter model from the prefix system, these strategies prevent resource bottlenecks and enable optimal throughput.

Resource allocation sensitivity. Figure 17 shows the Pareto frontier for different resource allocation policies in C-II, including both collocated and disaggregated placement plans. For collocated plans, the maximum QPS/chip can vary by up to 52.5× if insufficient resources are allocated to high-workload stages, when other stages have surplus capacity. For example, in the collocated plan (Figure 17a), imbalanced resource distribution across the encoder and prefix stages leads to underutilization of available accelerators, limiting throughput. This effect may amplify to 64.1× QPS/chip difference for disaggregated plans, as disaggregated stages rely heavily on precise balancing to maximize performance. Tailoring resource
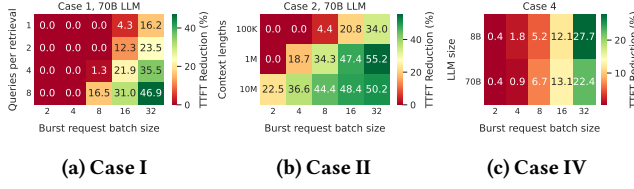
Figure 18: TTFT latency reduction by micro-batching.

distribution to the specific demands of each stage is essential for optimizing both latency and throughput in RAG systems.

Impact of micro-batching on TTFT latency. The effectiveness of micro-batching is determined by the throughput sensitivity to batch sizes at each pipeline stage. Figure 18 compares the impact of micro-batching on TTFT reduction across the case studies. For C-II (Figure 18b), micro-batching is effective even with a small batch size of two, reducing TTFT by 22%. This is because both the encoding and prefix stages are computationally intensive, achieving reasonable throughput even with smaller batch sizes. With larger batches of 32, the TTFT reduction increases further to 55% for 1M tokens. In C-I (Figure 18a), micro-batching only becomes effective with larger batch sizes, such as eight or 16. This inefficiency at smaller batch sizes arises from the vector search system, where reducing the query batch size below 16 fails to improve latency. However, with batch sizes increasing to 32, micro-batching still achieves a significant latency reduction of 46% for eight queries per vector. For C-IV (Figure 18c), TTFT reduction is moderate, with a maximum improvement of approximately 25% at a batch size of 32. This modest improvement is primarily due to the query rewriter decoding stage, which exhibits little latency reduction with smaller sequence batch sizes.

8 Additional Related Work

RAG performance optimization. As an emerging research area, RAG performance optimization remains underexplored, with existing studies targeting specific configurations. For instance, retrieval acceleration [43] is effective when retrieval costs dominate, document prefetching [44, 106] benefits iterative retrievals, and prefix state caching [46, 99] is efficient when the length ratio of prefix-to-decode is high. If these techniques are adopted, the workload distribution within a RAG system evaluated by RAGO is expected to shift. For example, retrieval acceleration [43] will shift the workload toward being more inference-bound. By contrast, caching KV states of retrieved documents [46, 99] will increase the importance of retrieval and decoding performance. Additionally, supporting iterative retrievals through data prefetching [44, 106] will reduce decoding engine idleness during retrieval operations.

LLM and retrieval optimization. Extensive research has been devoted to optimizing LLM systems and their underlying hardware [18, 54, 58, 65, 78, 80, 100, 102, 105, 109, 110]. Similarly, significant efforts have focused on enhancing retrieval efficiency on modern hardware, spanning product-quantization-based ANN algorithms [42, 47, 60, 70] and graph-based approaches [32, 41, 103, 107].

However, the complexity and heterogeneity of RAG pipelines far surpass those of LLM-only or retrieval-only systems, rendering direct extensions of these systems inadequate for efficient RAG serving.

9 Conclusion and Future Outlook

This work represents an early exploration of RAG through a systems lens, establishing a foundation for this rapidly evolving field. Our contribution, RAGSchema, provides a structured abstraction for RAG serving, facilitating systematic workload characterization and bridging the gap between algorithms and system design. Leveraging RAGSchema, we proposed RAGO,a system optimization framework that delivers up to a 2× improvement in QPS per chip and a 55% reduction in TTFT compared to a strong baseline.

As the field advances, our characterization results can guide the co-design of future systems and RAG workloads. For instance, our findings highlight that retrieval can become a bottleneck in certain RAG paradigms, particularly at hyperscale, underscoring the need for further retrieval optimizations. Moreover, with multiple model components in RAG pipelines, efficient support for collocated models on accelerators will be increasingly critical.

While RAGO demonstrates promising progress, it marks an initial step in comprehensive RAG workload evaluation. Future extensions of RAGO could explore innovative system and architecture designs. For example, offloading smaller inference models to host CPUs alongside retrieval could help mitigate rising XPU costs. Additionally, scaling to extremely large and complicated RAG systems introduces challenges related to a broader optimization search space and additional efficiency metrics, such as energy and cost efficiency. We leave these investigations to future work.

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